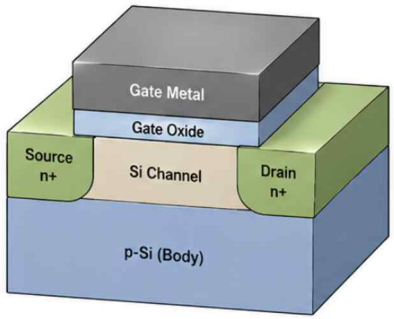
반도체공학회
ISE The Institute of Semiconductor Engineers

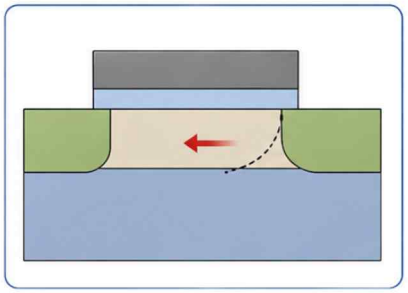
Dual-Metal Gate를 이용한 미세 MOSFET의 SCE 및 Leakage Current 개선 효과분석

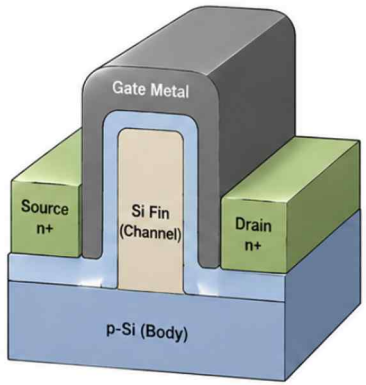
숭실대학교 차세대반도체학과 특별세션 | 이선재 | 주상현

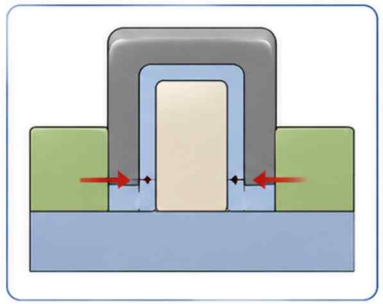
기술 동향 분석 Work Function Engineering의 필요성

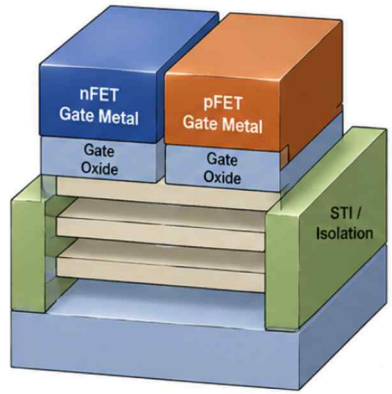
Planar MOSFET → **FinFET / GAA** → **Nanosheet / CFET**

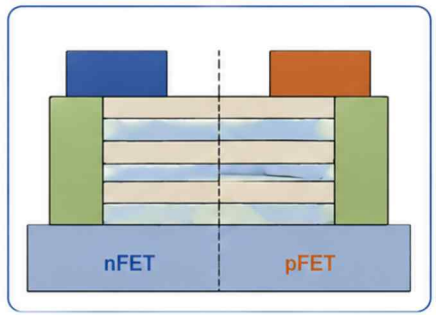












기술 동향 분석 Work Function Engineering의 필요성 (선행연구 분석)

A Review of the Gate-All-Around Nanosheet FET Process Opportunities

by Sagarika Mukesh †,‡ and Jingyun Zhang *,‡

IBM Research Albany, Albany, NY 12203, USA
* Author to whom correspondence should be addressed.
† Current address: 257 Fuller Road, Suite 3100, Albany, NY 12203, USA.
‡ These authors contributed equally to this work.

Electronics **2022**, *11*(21), 3589; **https://doi.org/10.3390/electronics11213589**

Submission received: 3 October 2022 / Revised: 27 October 2022 / Accepted: 2 November 2022 / Published: 3 November 2022

5. Enabling Multiple Threshold Voltages

The ability to co-integrate multiple threshold voltages (V_T) is a key requirement for a technology to become an industry standard. Given the unique architecture of GAA FETs, the space for depositing the work function metals is limited as depicted in **Figure 7**. The replacement metal gate process only leaves the space between the Si channels and inner spacers open—to be filled with the work function metals as per technology requirements. This space, also known as T_{sus} (refer **Figure 2**), can be controlled by controlling the thickness of SiGe layer grown during the nanosheet stack development module, but is nevertheless highly constrained, and must be engineered carefully to meet the industry standards for device offerings.

5.1. Integration

Two different approaches are proposed to accommodate multi-V_T offerings in GAA FETs—(1) WFM modification and (2) T_{sus} modification [20]. A process flow overview for WFM modification is presented in **Figure 8**. One of the challenges highlighted by the integration sequence for V_T modulation is that large W_{sheet} adds process challenges for WFM etch back when WFM is pinched-off between Si channels. To overcome this, ref. [21] proposed filling the space between sheets with a sacrificial material that is easy to etch, selectively opening one of the FETs, and etching away the already deposited work-function metal. This scheme is agnostic of p-type or n-type WFM, and enables both PG (p-FET first) and MY (n-FET first) schemes. This same process can be repeated to achieve different sets of work function metals or to achieve a different stack with more than two WFMs.

핵심 요구사항
multi-Vt 구현

→

WFM modification

→

공정 난이도 높음

기술 동향 분석 Work Function Engineering의 필요성 (선행연구 분석)

Dual Material Gate Engineering to Reduce DIBL in Cylindrical Gate All Around Si Nanowire MOSFET for 7-nm Gate Length

PHYSICS OF SEMICONDUCTOR DEVICES | Published: 02 November 2020
Volume 54, pages 1490–1495 (2020) Cite this article

Abstract

In this work, drain current I_D for 7-nm gate length dual-material (DM) cylindrical gate all around (CGAA) silicon nanowire (SiNW) has been studied and simulation results are reported using Silvaco ATLAS 3D TCAD. In this device, we consider the non-equilibrium Green's function (NEGF) approach and self-consistent solution of Schrödinger's equation with Poisson's equation. The splitting of conduction in multiple sub-bands has been considered and there is no doping in the channel region. The effect of DM gate engineering (variation of screen gate and control gate length having different work function) for SiNW channel with 2-nm radius and gate oxide (SiO_2) thickness of 0.8 nm on I_D have been studied. It was found that DM gate engineering reduces drain-induced barrier lowering (DIBL) but it also slightly increases sub-threshold slope (SS). This work has obtained small DIBL (~54 mV/V), small SS (~68 mV/dec), and higher I_{On}/I_{Off} (~4×10^8) ratio as compared to literature concerning the inversion mode devices. The smallest DIBL is obtained when control gate length is the highest, and vice versa. With increase in control gate length, there is also increase in both I_{On} and I_{Off} but I_{On}/I_{Off} ratio decreases.

Dual-material gate → **DIBL 저감** → **Gate 비율에 따른 차이 존재**

기술 동향 분석 Work Function Engineering의 필요성

Vt Fine-Tuning in Multi-Vt Gate-All-Around Nanosheet nFETs Using Rare-Earth Oxide-Based Dipole-First Gate Stack Compatible with CFET Integration

Publisher: IEEE Cite This PDF

H. Arimura ; H. Mertens ; J. Franco ; L. Lukose ; W. Maqsood ; S. Brus All Authors

Threshold Voltage Variability in Nanosheet GAA Transistors

Publication » *Article* • 01 Oct 2019 •

Publisher: Institute of Electrical and Electronics Engineers (IEEE) • Journal: IEEE Transactions on Electron Devices, volume 66, pages 4,433-4,438 (issn: 0018-9383, eissn: 1557-9646, Copyright policy)

Authors: *P. Harsha Vardhan; null Amita; Swaroop Ganguly; Udayan Ganguly;*

DOI: 10.1109/ted.2019.2933061

V_tTuning of Split-Gate GeSi Nanosheet CFETs With Dual Work Function Metals

January 2025 · IEEE Transactions on Electron Devices PP(99):1-6

DOI:10.1109/TED.2025.3592634

Authors:

Ying-Qi Liu Bo-Wei Huang Chun-Yi Cheng

Wei-Jen Chen

Gate Geometry → 확장 → **전기적 특성 제어**

기술 동향 분석 Work Function Engineering의 필요성

V_tTuning of Split-Gate GeSi Nanosheet CFETs With Dual Work Function Metals

January 2025 · IEEE Transactions on Electron Devices PP(99):1-6

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Authors:

Ying-Qi Liu Bo-Wei Huang Chun-Yi Cheng

Wei-Jen Chen

최신 동향에서도 여전히 연구 존재

연구 방향성 계획 수립

Dual-metal Gate → Planar MOSFET으로 실험

소자 구조에 따른 물리적 효과 검증 목적

1	DIBL과 Ioff 완화 가능성 검증
2	구조 변화에 따른 부가 문제 재검토
3	Gate 비율 변화에 따른 Trade-off 분석

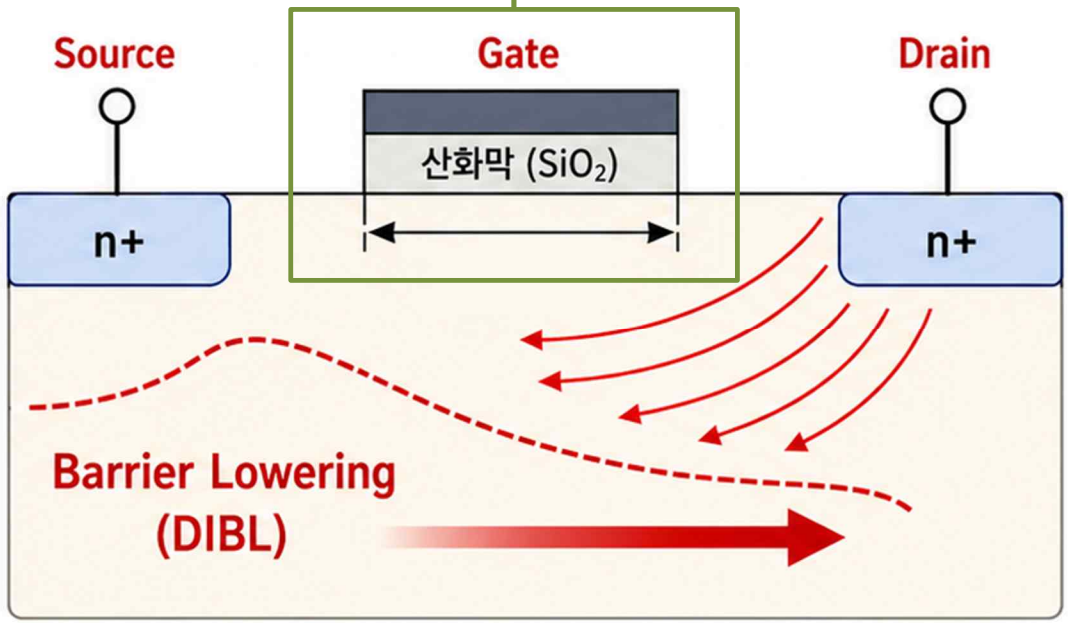
문제점 제시 미세 MOSFET의 누설전류 증가 문제

Gate length 감소

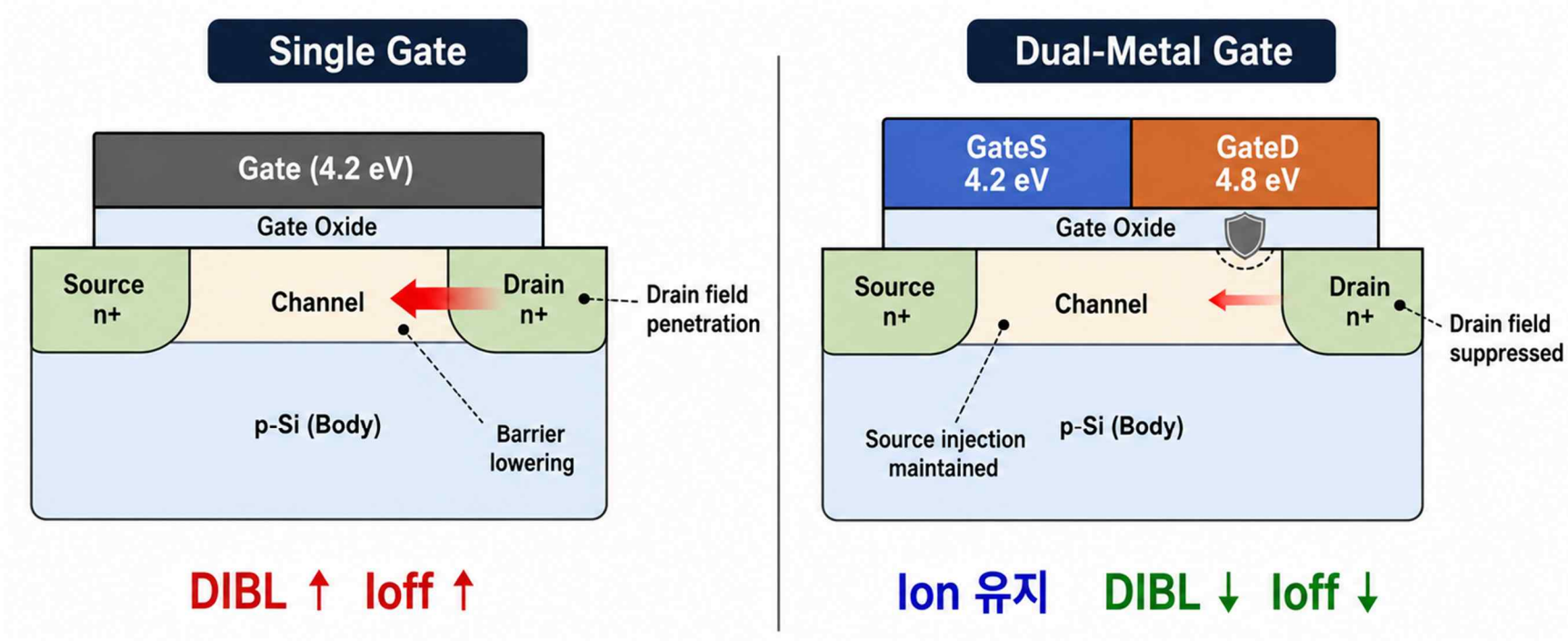
Short-channel effect
(SCE)

Ioff 증가

DIBL 증가
(뒤에서 추가설명)



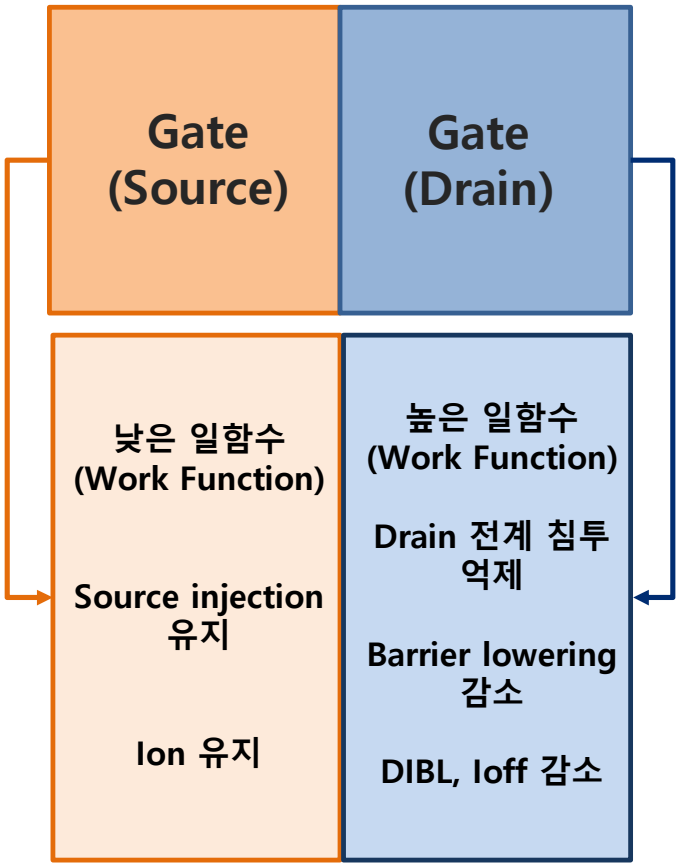
해결방안 Dual-Metal Gate를 이용한 Short-Channel Effect 억제



Dual-Metal Gate

- Source (낮은 일함수 gate) — 전자 장벽 낮게 유지(Ion 유지)
- Drain (높은 일함수 gate) — Drain 전계 침투 억제(Ioff 감소)

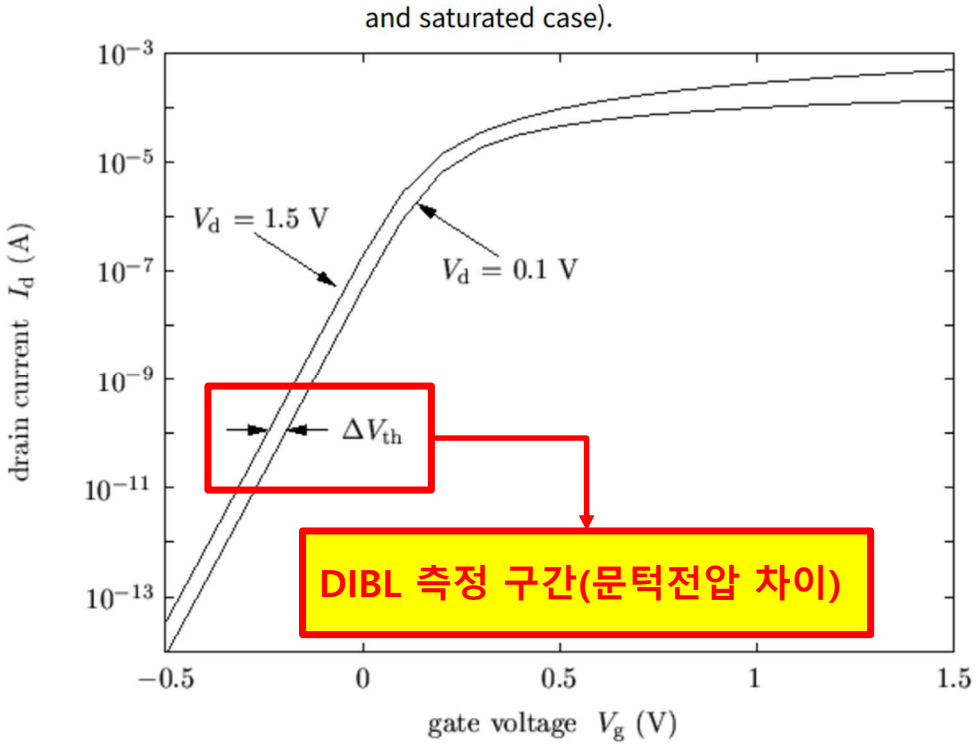
가설 설정 Dual-Metal Gate 적용 시 전기적 특성 개선 예측



지표	예상 변화	이유
Ion	유지(소폭감소)	Source 측 Low-Wf으로 Carrier injection 유지
Ioff	감소	Drain 측 barrier lowering 억제
DIBL	감소	Drain 전계가 Source barrier에 미치는 영향 감소
SS	유지(안정화)	Channel barrier 제어력 향상
Ion/Ioff	증가	Ion의 손해보다 Ioff의 이득 효과가 클 것으로 예상

* 단일 금속으로 gate를 형성했을 때보다 다음과 같은 성능 향상을 기대할 수 있다.

DIBL DIBL 정의 및 TCAD 평가 방법



Drain 전압 증가 → Source-Channel Barrier 저하 → 문턱전압 변화

DIBL이 큼 → Drain 전계 영향 큼 → off-state leakage current 증가

$$DIBL(mV/V) = \frac{|Vth,Low - Vth,High|}{(Vd,High - Vd,Low)}$$

SDevice 평가 과정

Vd_Low 조건에서 Id-Vg sweep → Vd_High 조건에서 Id-Vg sweep →
각 curve에서 Vth 추출 → 위 식을 사용해 DIBL 계산

https://www.iue.tuwien.ac.at/phd/stockinger/node15.html

TCAD SProcess 구현 Dual-Metal Gate MOSFET 공정 구현

SimpleMOS 기반
(nMOS)

↓

GateS/GateD
형성

↓

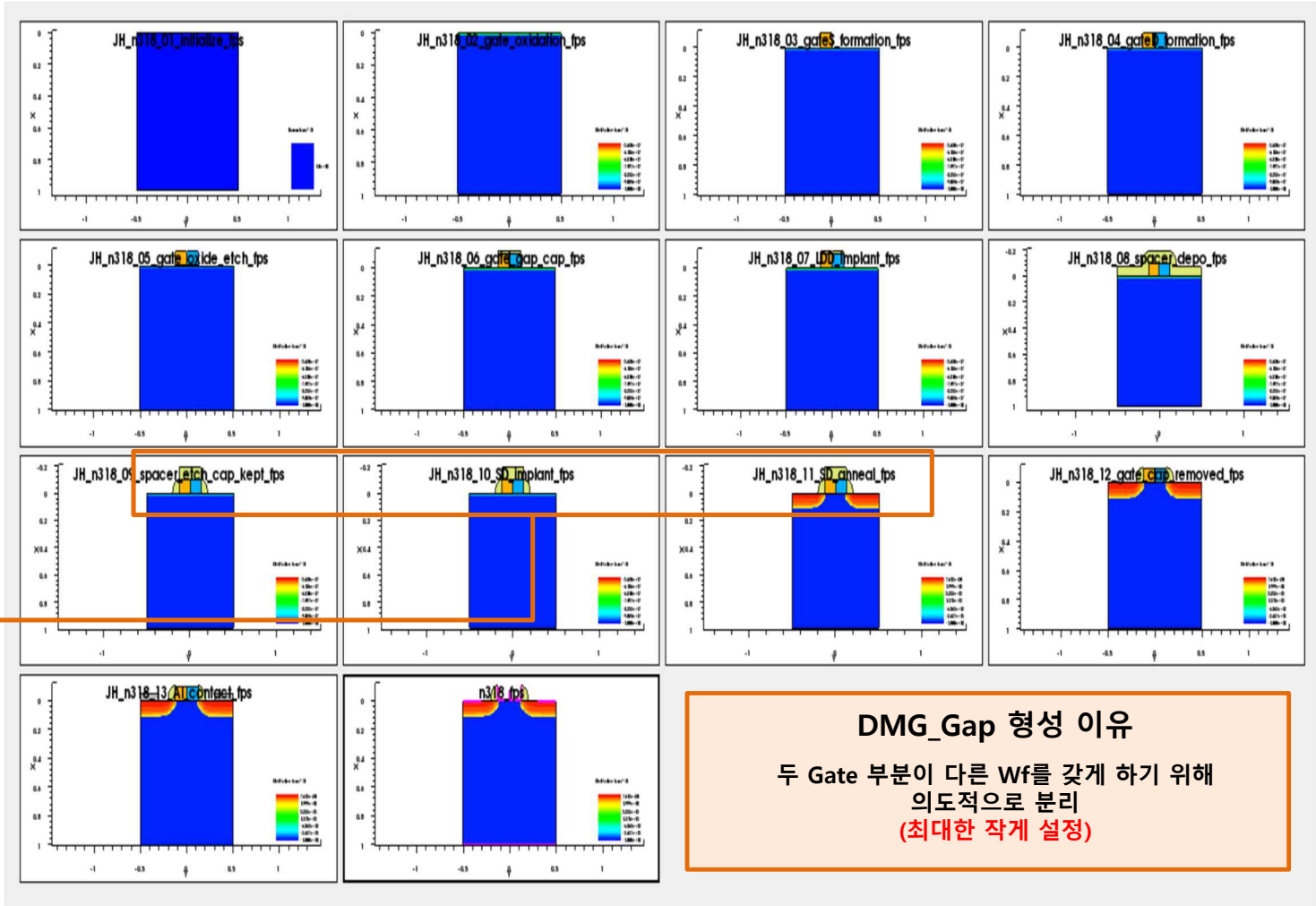
DMG_Gap 형성
(Gate 간 빈공간 형성)

↓

Gap 보호 cap 형성
(도핑 침투 방지)

↓

도핑 후 cap 제거



DMG_Gap 형성 이유

두 Gate 부분이 다른 Wf를 갖게 하기 위해
의도적으로 분리
(최대한 작게 설정)

1차 검증 Lg = 0.25 μm 기준 소자에서 Dual-Metal Gate 효과 검증 및 최적화

Lg=0.25 baseline

Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.25	1.00E+17	0.1	5.00E+13	0.001	15	15	1.00E+15	4.2	4.2	0.0016	400.77	67.73	2.79E-04	2.02E-09	138086.7
0.25	5.00E+17	0.1	5.00E+13	0.001	15	15	1.00E+15	4.2	4.8	0.0016	328.43	68.78	2.56E-04	1.15E-16	2.23E+12

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용

감소 | 유지 | 유지 | 감소 | 증가

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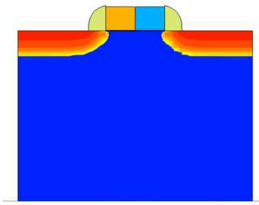

*gate 및 spacer size는 유지

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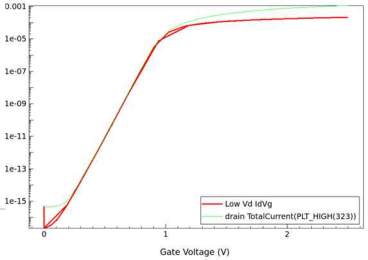

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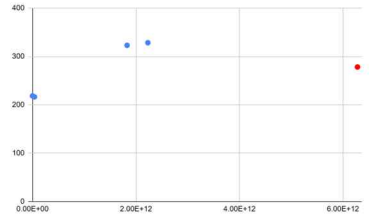

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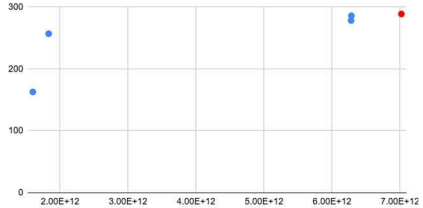

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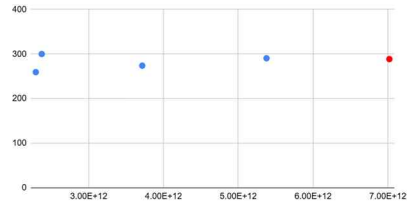

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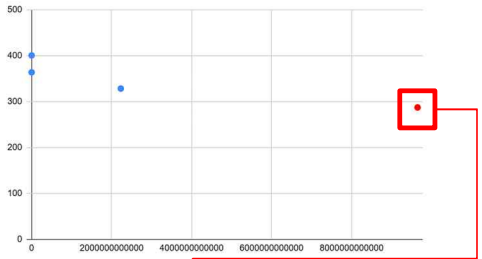

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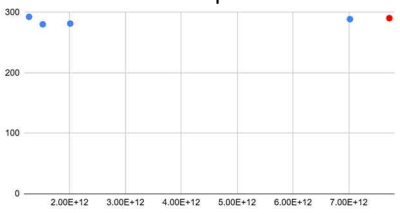

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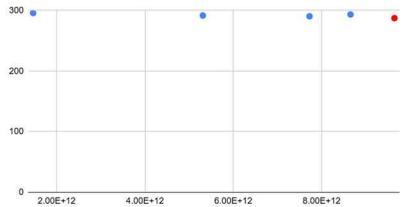

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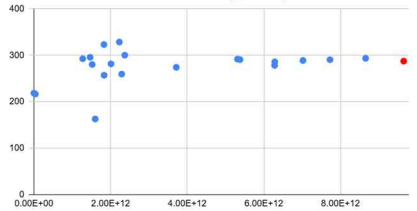

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Lg=0.25 최적화

Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.25	1.00E+18	0.1	7.00E+13	0.001	15	5	3.00E+15	4.2	4.2	0.0016	363.86	69.85	2.39E-04	8.45E-11	2.83e+06
0.25	1.00E+18	0.1	7.00E+13	0.001	15	5	1.00E+15	4.2	4.8	0.0016	287.34	70.73	2.16E-04	2.24E-17	9.65e+12

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용

감소 | 유지 | 유지 | 감소 | 증가

2차 검증 Lg = 0.1 μm 기준 소자에서 Dual-Metal Gate 효과 재검증 및 최적화

Lg=0.1 baseline

Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.1	5.00E+17	0.1	5.00E+13	0.001	10	10	5.00E+14	4.2	4.2	0.0016	224.45	69.59	5.21E-04	1.69E-08	30836.31
0.1	5.00E+17	0.1	5.00E+13	0.001	10	10	5.00E+14	4.2	4.8	0.0016	206.24	76.59	4.84E-04	2.16E-15	2.24E+11

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용

감소 | 유지 | 유지 | 감소 | 증가

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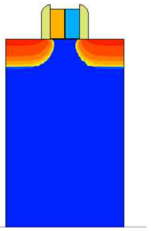

*gate 및 spacer size는 유지

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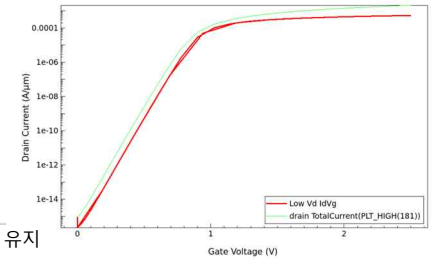

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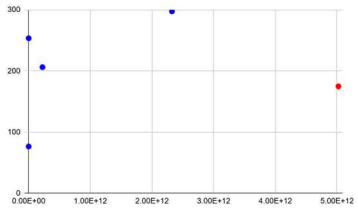

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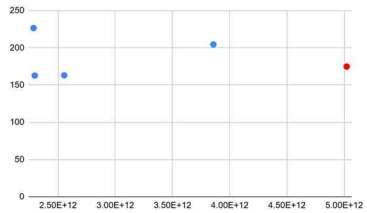

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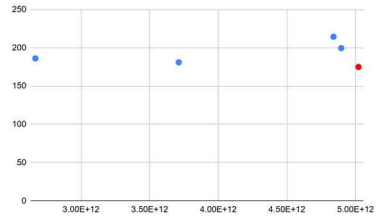

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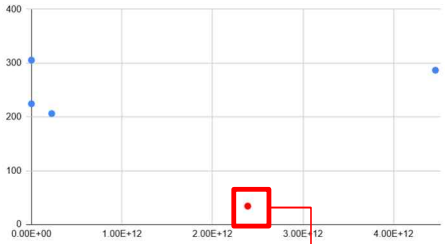

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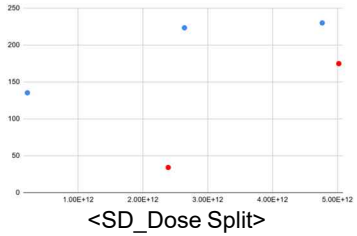

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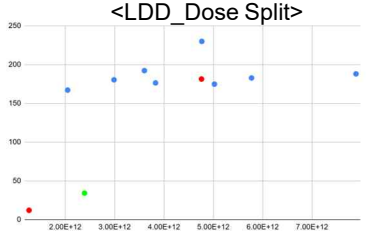

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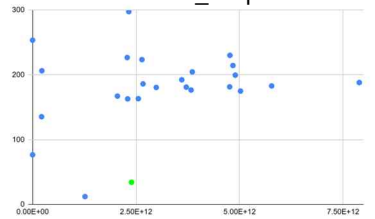

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감소 | 유지 | 유지 | 감소 | 증가

Lg=0.1 최적화

Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.1	1.00E+18	0.1	5.00E+13	0.001	10	10	1.00E+15	4.2	4.2	0.0016	305.63	70.3	5.86E-04	1.31E-09	447270.12
0.1	1.00E+18	0.1	5.00E+13	0.001	10	10	1.00E+15	4.2	4.8	0.0016	34.16	73.8	5.36E-04	2.24E-16	2.39E+12

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용

3차 검증 Lg = 0.028 μm 고도 미세소자에서 Dual-Metal Gate 적용성 검증

Lg=0.028 baseline

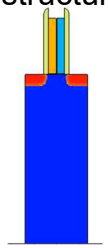
Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.028	5.00E+18	0.1	5.00E+12	0.001	3	3	1.00E+14	4.2	4.2	0.0016	274.4	81.44	6.19E-04	1.70E-11	3.64E+07
0.028	5.00E+18	0.1	5.00E+12	0.001	3	3	1.00E+14	4.2	4.8	0.0016	28	85.44	5.71E-04	1.49E-16	3.84E+12

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용

* 미세소자 구현 시에 구조가 붕괴되지 않는 baseline을 탐색하였음

감소 | 유지 | 유지 | 감소 | 증가

<structure>



*gate 및 spacer size는 유지

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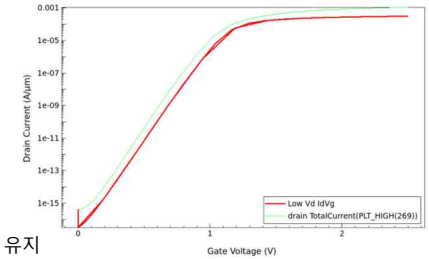
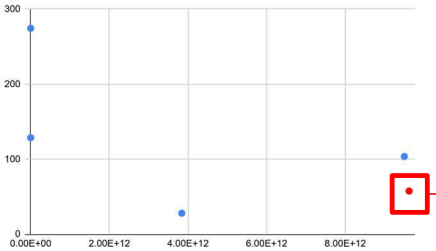


<최적화 판단 기준 : Ion/Ioff – DIBL 그래프를 통한 최적점 확인>



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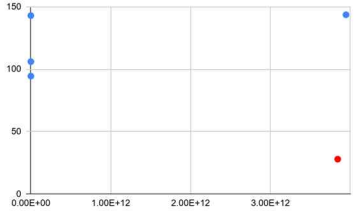

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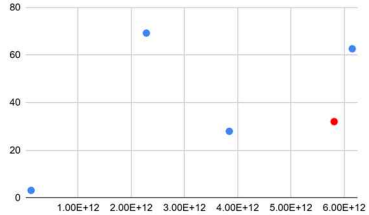
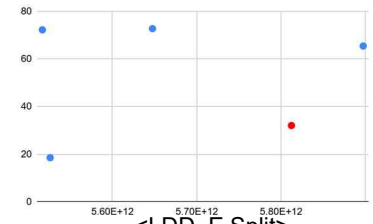


<LDD_Dose Split>



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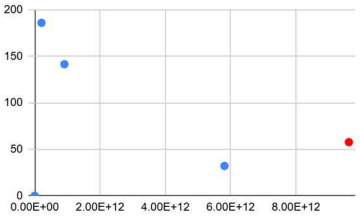

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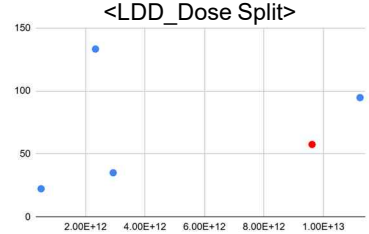

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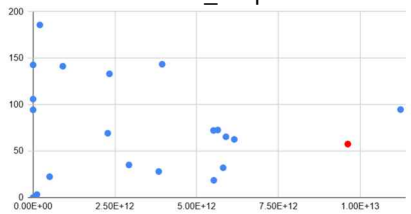

<전체 Data 비교>

Lg=0.028 최적화

Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.028	5.00E+18	0.1	1.00E+12	0.001	3	3	5.00E+13	4.2	4.2	0.0016	128.67	79.98	3.34E-04	3.78E-12	8.85E+07
0.028	5.00E+18	0.1	1.00E+12	0.001	3	3	5.00E+13	4.2	4.8	0.0016	57.58	83.41	3.16E-04	3.28E-17	9.62E+12

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용

감소 | 유지 | 유지 | 감소 | 증가

결과

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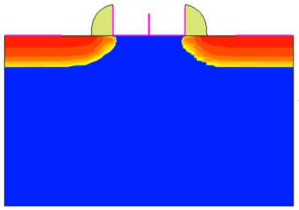

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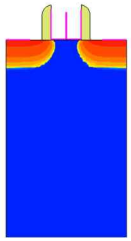

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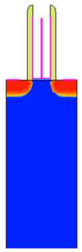
SCE 억제 효과 확인

<structure>



<Lg=0.028>

미세소자 수준에서도
Single-Metal Gate 대비 Dual-Metal Gate가
가설과 같은 효율 경향성을 보임을 확인

- DIBL 감소
- Ion/Ioff 비율 증가
- SS 안정성 유지

<오차 가능성 고찰>

일부 조건에서 고전압 문턱전압이 저전압 문턱전압보다 크게 추출되는 현상 발생

- 일반적인 DIBL 방향과 반대
- Vtgm 기반 Vth 추출 방식으로 인한 오차로 추정
- DIBL 절대값 비교
- DIBL 특이값은 배제 → SS, Ioff, Ion/Ioff 함께 고려

Lg=0.1 최적화

Dose	Wf_S	Wf_D	tox	DIBL(mV/V)
:+15	4.2	4.2	0.0016	305.63
:+15	4.2	4.8	0.0016	34.16

<Lg=0.1 최종값>

0.028 baseline

Wf_S	Wf_D	tox	DIBL(mV/V)
4.2	4.2	0.0016	274.4
4.2	4.8	0.0016	28

8 V High = 0.7 에서 측정

<Lg=0.028 baseline>

신뢰성 낮은 Data, 경향성만 확인

DIBL 약 90% 감소

Figures on Slides 1–2 and the TCAD simulation codes, including SProcess, SDevice, and SVisual scripts, were generated with the assistance of ChatGPT by OpenAI. The generated materials were reviewed, modified, and applied by the authors for this project.

문제점 발견

tox
0.0016

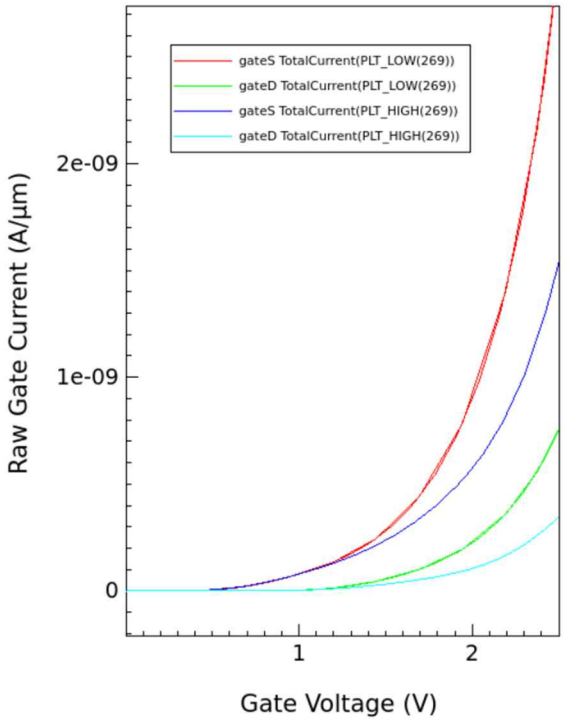
< = 1.6nm >

매우 얇은 산화막 두께

→ 미세소자일수록 Gate 누설 전류가 치명적

Total Leakage 증가 가능성 존재

<Ig-Vg Curve>



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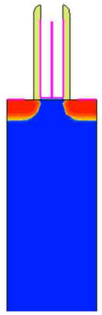

<Lg=0.028>

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<Lg=0.028>

Lg=0.028 최적화

Lg	NWell	GOxTime	LDD_Dose	DMG_Gap	LDD_E	SD_E	SD_Dose	Wf_S	Wf_D	tox	DIBL(mV/V)	SS	Ion	Ioff	Ionloff
0.028	5.00E+18	0.1	1.00E+12	0.001	3	3	5.00E+13	4.2	4.2	0.0016	113.63	82.1	2.10E-04	2.22E-11	9.45E+06
0.028	5.00E+18	0.1	1.00E+12	0.001	3	3	5.00E+13	4.2	4.8	0.0016	37.65	85.42	2.05E-04	2.90E-16	7.05E+11

- V_Low = 0.08, V_High = 0.7 에서 측정
- SS, Ion, Ioff 값은 V_Low 데이터 기준으로 사용
- 소자 비율 추가 개선 추가실험으로 인해 전체 Data 값이 이전 page와 변경되어 있음

Ig / Total Leakage Data

Wf_S	Wf_D	IgS_Off	IgD_Off	IgTotal_Off	IgS_On	IgD_On	IgTotal_On
4.2	4.2	3.33E-19	1.56E-15	1.56E-15	2.99E-09	2.91E-09	5.90E-09
4.2	4.8	1.02E-24	1.05E-21	1.05E-21	2.95E-09	7.58E-10	3.71E-09

각각의 Gate로 누설되는 전류 확인

개선 시도 High-K 구조 적용

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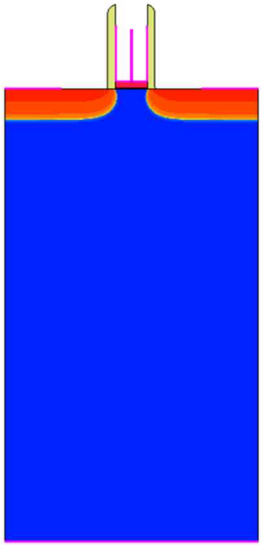


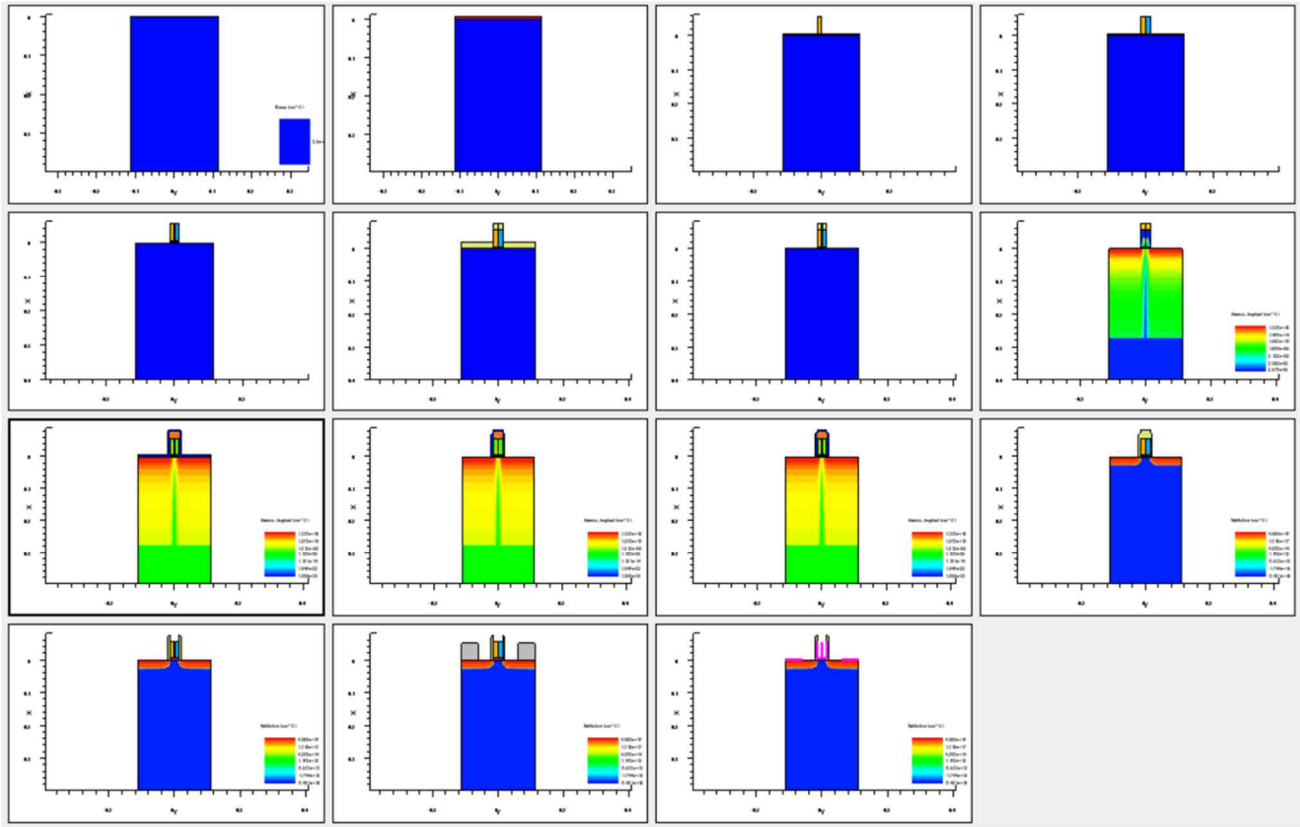
<Lg=0.028, High-K>

기존 Dual-Metal Gate
공정 기반

EOT = 1.6 nm 유지
HfO_2 소재 적용

실제 절연막 두께
→ 6.14 nm

기존 산화막 대비
실제 두께 283.75% 증가



개선 시도 High-K 구조 적용

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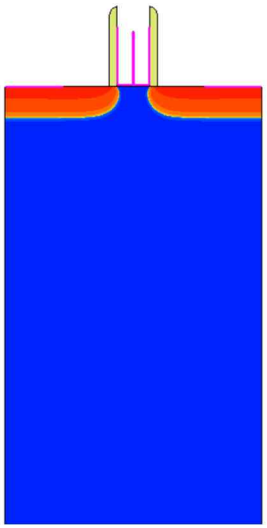

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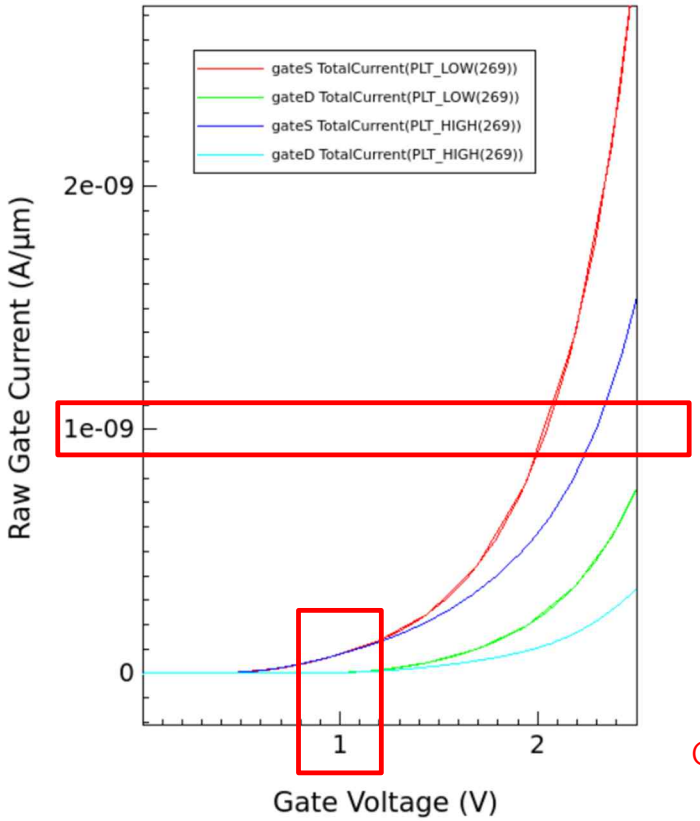
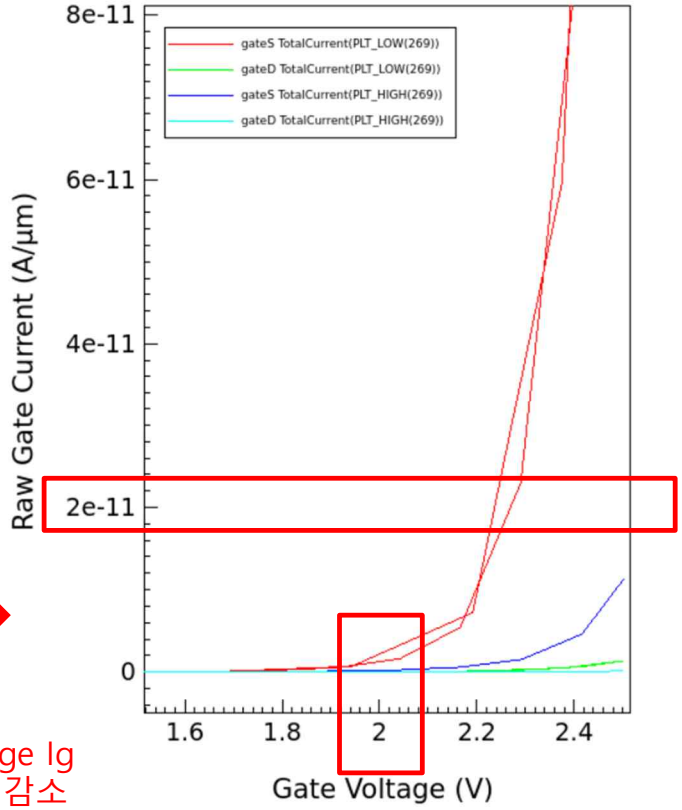


Gate Leakage Ig
약 99.40% 감소



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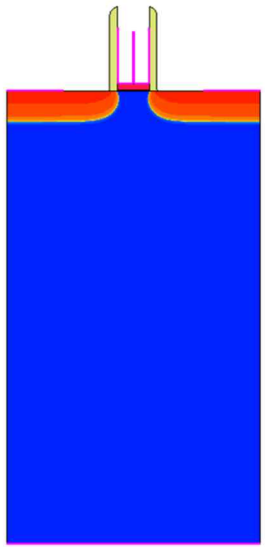
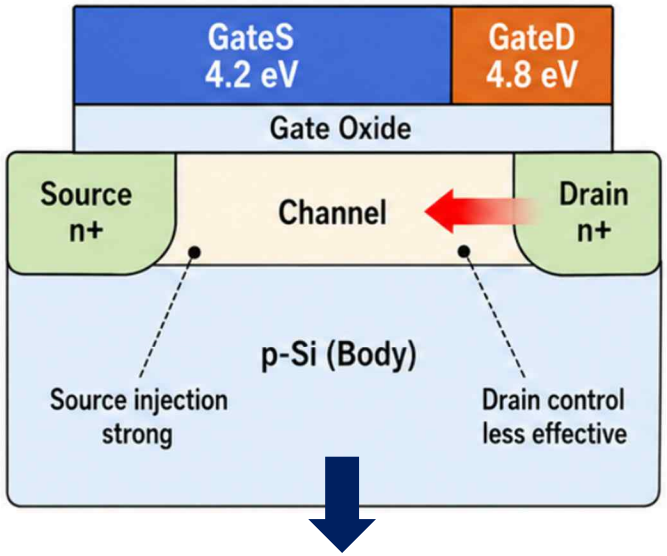


<Lg=0.028, High-K>

DMG 비율 변화 실험 설계

GateS Longer

Gate Ratio (S:D) ≈ 60:40

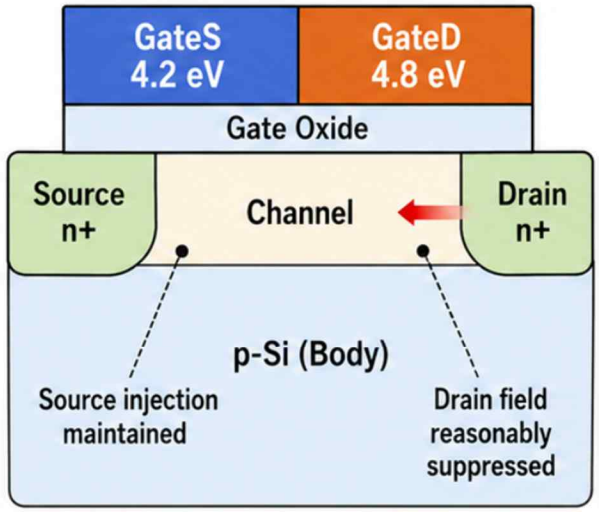


전자 주입 장벽 낮게 유지

DIBL/Ioff 증가 가능

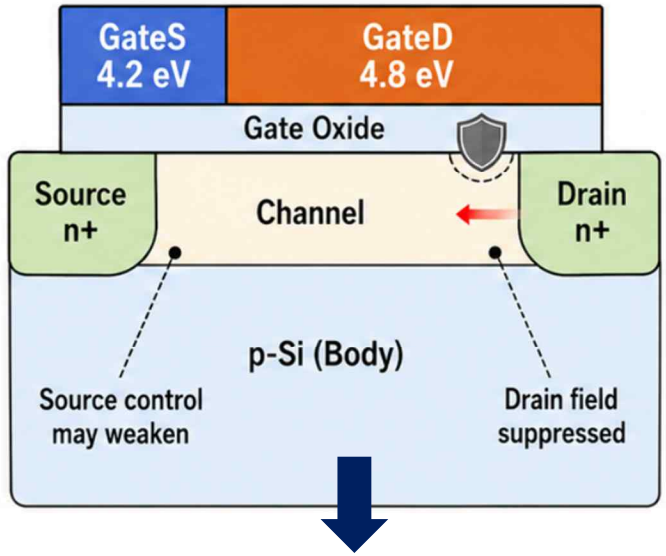
Balanced Ratio (50:50)

Gate Ratio (S:D) = 50:50



GateD Longer

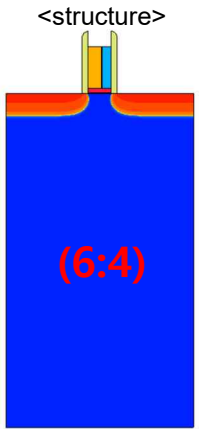
Gate Ratio (S:D) ≈ 40:60

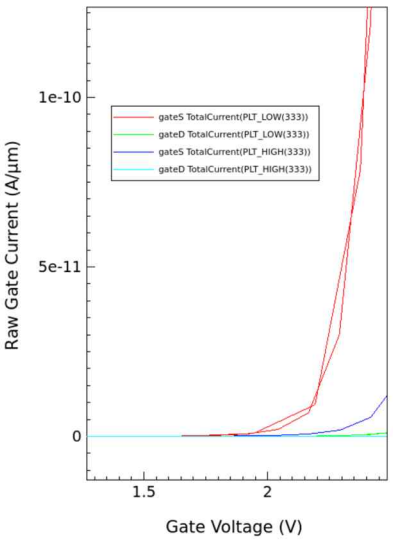


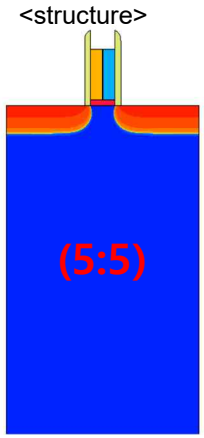
Drain 전계 침투 억제 강화

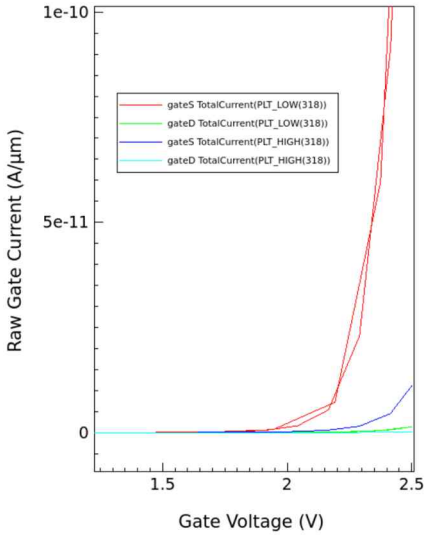
Ion 감소 및 SS trade-off 가능

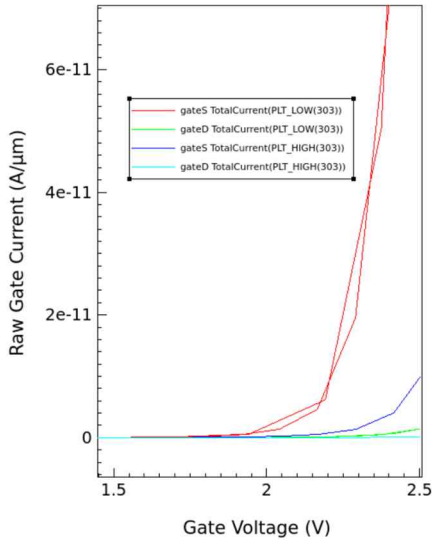
DMG 비율에 따른 추출값 확인 (Source Gate : Drain Gate)

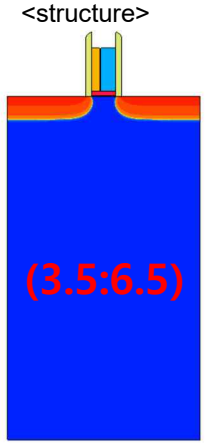


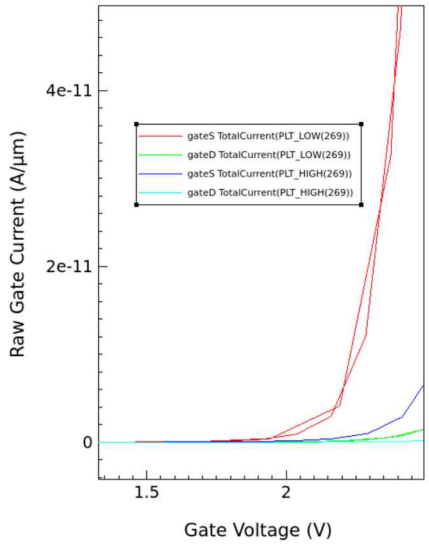












DMG 비율에 따른 추출값 비교 (Source Gate : Drain Gate)

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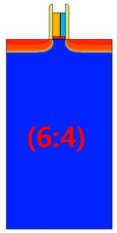
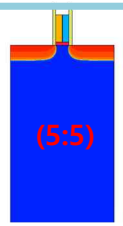


Gate 비율 6:4 Raw Data

Wf_S	Wf_D	EOT	DIBL(mV/V)	SS	Ion	Ioff	Ionloff	IgS_Off	IgD_Off	IgTotal_Off	IgS_On	IgD_On	IgTotal_On
4.2	4.8	0.0016	19.47	86.03	1.85E-04	2.03E-15	9.12E+10	4.94E-28	9.84E-28	1.48E-27	2.87E-10	1.20E-12	2.88E-10

가장 높은 Ion / 그러나 Ioff 값과 SS 수치 저하



가장 균형성이 좋다고 판단

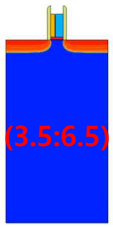
Gate 비율 5:5 Raw Data

Wf_S	Wf_D	EOT	DIBL(mV/V)	SS	Ion	Ioff	Ionloff	IgS_Off	IgD_Off	IgTotal_Off	IgS_On	IgD_On	IgTotal_On
4.2	4.8	0.0016	22.35	84.85	1.84E-04	4.30E-16	4.29E+11	5.24E-29	9.90E-28	1.04E-27	2.16E-10	1.36E-12	2.17E-10

Gate 비율 4.5:5.5 Raw Data

Wf_S	Wf_D	EOT	DIBL(mV/V)	SS	Ion	Ioff	Ionloff	IgS_Off	IgD_Off	IgTotal_Off	IgS_On	IgD_On	IgTotal_On
4.2	4.8	0.0016	2.57	84.44	1.84E-04	2.88E-16	6.38E+11	1.88E-29	4.60E-28	4.79E-28	1.81E-10	1.44E-12	1.83E-10

신뢰성 낮음



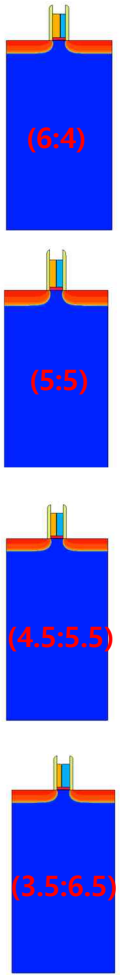
Gate 비율 3.5:6.5 Raw Data

Wf_S	Wf_D	EOT	DIBL(mV/V)	SS	Ion	Ioff	Ionloff	IgS_Off	IgD_Off	IgTotal_Off	IgS_On	IgD_On	IgTotal_On
4.2	4.8	0.0016	56.89	83.94	1.83E-04	2.08E-16	8.82E+11	3.78E-30	3.56E-28	3.59E-28	1.15E-10	1.54E-12	1.17E-10

SS, Ion, Ioff 값이 가장 우수 / DIBL 악화

결과

<structure>



Drain Gate
비율 증가

DIBL(mV/V)
19.47

높은 Ion / 그

DIBL(mV/V)
22.35

DIBL(mV/V)
2.57

신뢰성 낮음

DIBL(mV/V)
56.89

SS, Ion, Ioff

DIBL 증가 경향성
(신뢰성 낮은 Data 제외)

SS/Ion/Ioff 감소 경향성

SS	Ion	Ioff
86.03	1.85E-04	2.03E-15

러나 Ioff 값과 SS, DIBL 수치

SS	Ion	Ioff
84.85	1.84E-04	4.30E-16

SS	Ion	Ioff
84.44	1.84E-04	2.88E-16

SS	Ion	Ioff
83.94	1.83E-04	2.08E-16

원인 고찰

DIBL
Trade-off 의 영향으로 신뢰성 낮음

SS
Drain Gate 영역 확대 →
channel barrier 제어가 일부 개선

Ion
Source Gate 영역 감소 →
carrier injection 유지 효과가 약화

Ioff
Drain Gate 영역 확대 →
drain 전계 침투 및 off-state leakage 억제

결론

반도체공학회 ISE The Institute of Semiconductor Engineers

결과 1	**DMG : DIBL/Ioff 감소 경향성** Source/Drain gate WF 역할 분리 효과 확인
결과 2	High-K 적용으로 Gate Leakage 해결
결과 3	Gate 비율 변화에 따른 Trade-off 확인
한계점	실제 GAA/CFET 적용을 위해서는 dual-WFM 형성 공정 개선 필요
	선택적 증착/식각, alignment, WFM variability 제어 필요

CFET Multi-Vt 및 저전력 logic 소자용 Work-Function Engineering으로 확장가능

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Q&A

숭실대학교 차세대반도체학과 특별세션 | 이선재 | 주상현